ELEN E4312
Fall 2007
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OP-AMP DESIGN PROJECT

Your company is investigating a custom low-cost, low power 1.8 GHz wireless communication system. The system is intended to transmit and receive data at a rate of 1Mb/s, and is to be designed in a 0.13μm SiGe BiCMOS technology. A simplified block diagram for the CU4312 quadrature wireless receiver is shown in Figure 1.

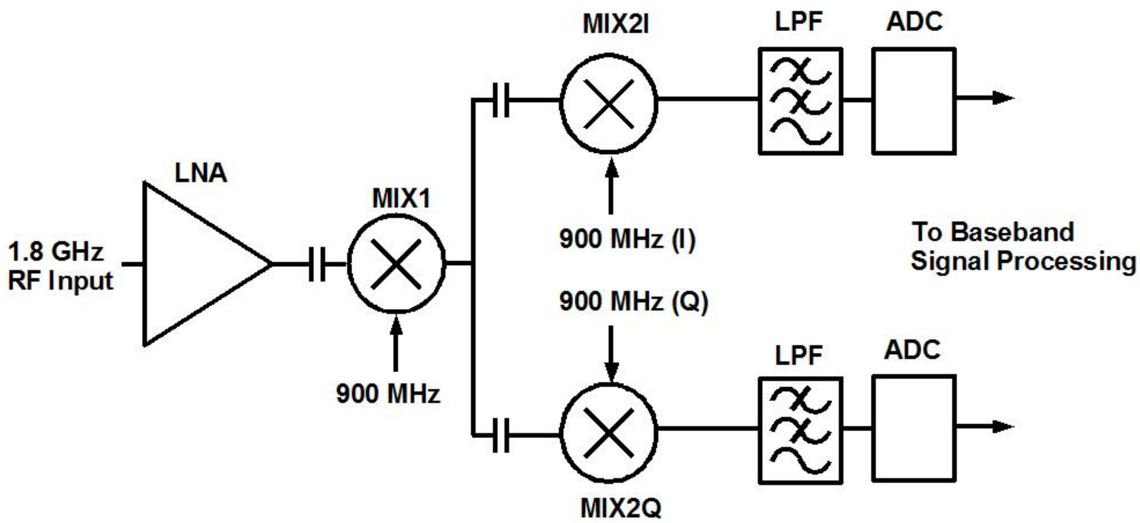

Figure 1: CU4312 Wireless Receiver Architecture.

The 1.8 GHz wireless signal is received by an antenna, amplified by a low-noise amplifier. The high-frequency signal is downconvertered to baseband using two mixers. Low-pass filters (LPF) on the in-phase (I) and quadrature-phase (Q) paths are used to remove unwanted tones or signals before the I/Q signals are fed to A/D converters (ADC) for baseband signal processing. ***Your group is responsible for the design of the low-pass filters.***

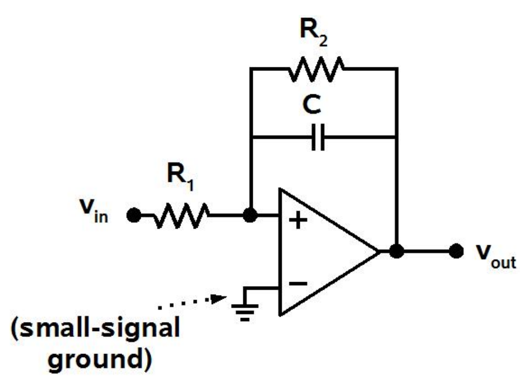

Figure 2: Proposed low-pass filter schematic.

A proposed schematic of the low-pass filter is shown in Figure 2. More information on this filter topology can be found in Chapter 12 of the Sedra & Smith textbook (in particular, see Figure 12.13). Based on system-level analysis provided by the system architect, it is decided that the 1st order low-pass filter must meet the following specifications.

Specification	Target
Gain	20 dB
Cutoff frequency (3dB)	1 MHz
Input resistance	>5kΩ

Table 1: Low-Pass Filter Specifications

The critical block in the low-pass filter is the operational amplifier. The op-amp has a single-ended output and should be designed to meet the following specifications.

Specification	Target
Gain	> 50 dB
Unity gain bandwidth	>20 MHz
Supply voltage	Standard: 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V (your choice)
Power consumption	TBD
Input Common-Mode Range	$V_{DD}/2 < V_{IN,CM} < V_{DD}$
CMRR	> 70 dB
I_{REF}	100 μA
Phase margin	> 45^o

Table 2: Operational Amplifier Specifications

Simulations should be run to ensure specifications are met at 0C, 27C (room temperature), and 100C. Moreover, the op-amp must meet specifications for supply voltage of +/- 10% of the nominal (e.g., 900mV to 1.1V for a nominal 1.0V supply, 3V to 3.6V for a nominal 3.3V supply. The unity gain bandwidth should be at least 20 MHz. A single 100μA reference current is available. All bias currents should be derived from this reference current. The power consumption should be low; however, you have some flexibility with this. You may choose any standard supply voltage to design this part: 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V (nominal).

All devices available in the 0.13μm SiGe BiCMOS technology are available to you. This means you may use all CMOS transistors in your design, or you may choose to incorporate bipolar npn devices in your design (note that pnp devices are not offered in this technology). Take care to avoid operating devices beyond their breakdown voltage. For SiGe HBTs, the V_{CE} of the device should not exceed 1.8V. For 0.13μm MOSFETs, the $|V_{GS}|$, $|V_{GD}|$, or $|V_{DS}|$ of the transistor should not exceed 1.2V. Hence, op-amp topology and device selection will dictate your supply voltage.

Grading: The project will be graded based on meeting the target specifications. However, design creativity is encouraged. You may be able to meet the design specifications with a simple two-stage CMOS op-amp, but exploring more complex op-amp topologies will most likely result in a higher grade. Sedra & Smith covers only the two-stage op-amp, as well as folded-cascode op-amps. It is recommended that you look to other textbooks or IEEE journal articles for ideas on more advanced op-amp topologies. The Johns & Martin textbook (see the course syllabus) presents several other op-amps with improved gain, high slew-rate, etc.

Bonus marks: Bonus marks will be given to the group with (1) the highest unity-gain bandwidth and (2) the lowest power consumption.

Working in pairs: You are supposed to work in pairs. If you do not have a partner, email the instructor as soon as possible. You need only hand in one report per pair. Both partners are expected to contribute about equally to the effort. If this is not the case for you and your partner, *you are asked to state, on the first page of your report, the approximate percentage of each partner's contribution*.

GUIDELINES FOR PROJECT REPORTS

Length limit: Same as that imposed for *brief* papers in the IEEE Journal of Solid-State Circuits; not more than about 1800 words, plus 5-8 figures. For typed reports, this corresponds to no more than six double-space typewritten pages, plus figures. Tables should be included that summarize the performance of your op-amp circuit and low-pass filter.

Style: Similar to that of brief papers in the above journal; see recent issues in the library for examples. Be concise and to the point; give important results, but avoid showing details of lengthy calculations. In general, write your report as if you were to submit it for publication in the above journal. This means, among other things, that the report should be self-sufficient; all important results from computer simulations should be transferred to the report (e.g., in the form of plots), so that the reader can get the picture without having to examine your computer printouts.

Supplemental material: Although the report should be self-sufficient, you should also submit supplemental material that will assist in evaluating your work. This material could include screen dumps and printouts. ***In addition, a spectre netlist must be submitted.***

Report copy: Your original report will not be returned. If you want, make a copy before you hand it in.

DUE DATE: November 28th at the beginning of lecture. ***No late reports can be accepted.***